R E M A R K S

Claims 5 and 7 have been canceled, without prejudice, therefore claims 1-4, 6 and 8-20 are currently pending. Independent claims 1 and 10 have been amended herein. Replacement sheets including amended FIGS. 1 and 3 have been attached in response to a drawing objection. Applicants respectfully request that the Examiner reconsider the patentability of the pending claims based on the following discussion.

Objection to the Drawings

The drawings have been objected to on the grounds that they do not show all of the claimed features in that separate input/output lines are not shown in FIGS. 1 and 3, and that they fail to show reference characters 306, 308, 310, 338, 340 and 346. With regard to the first grounds for objection, Figures 1 and 3 have been amended (via replacement drawings) to show separate lines. However, the second grounds for objection are not understood because original FIG. 3 includes reference characters 306, 308, 310, 338, 340 and 346 (which each represent multiplexers) in accordance with the text of the specification.

§ 102 Rejection

Claims 1-4, 6, 8 and 10 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Watari, U.S. Patent No. 4,894,708 (‘*Watari*’).

Independent claim 1, as amended, recites as follows:

selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor ***using a first selection signal;*** *and*

selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor ***using a second selection signal.***

Watari apparently refers to a manual process for redirecting signals over different input/output lines. *See e.g. Watari*, col. 3, ll, 23-43 (describing the need to connect terminals using repair wires). Thus, *Watari* does not teach automatically changing the input and output lines for receiving and sending a test signal (respectively) using selection signals. Accordingly, it is submitted that *Watari* does not teach (or even suggest) the subject matter of amended claim 1.

It is accordingly submitted that independent claim 1, as amended, and its dependent claims 2-4, 6, 8 and 10 are not anticipated by *Watari*. Withdrawal of the rejection of the claims 1-4, 6, 8 and 10 based on *Watari* is therefore respectfully requested.

§ 103 Rejections

Claims 5, 7 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watari* in view of Bombal et al., U.S. Patent No. 6,141,782 (‘*Bombal*’); and claims 11-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watari* in view of Evans, U.S. Published Patent Application No. 2003/0208713 (‘*Evans*’).

With regard to the first rejection of claims 5, 7 and 9 based on *Watari* and *Bombal*, it is submitted that *Bombal* does not cure the deficiencies of the *Watari* reference with respect to the

independent claim 1, upon which claims 5, 7 and 9 depend. The Office Action appears to rely on *Bombal* for the teaching of modifying select signals. It is noted however, that *Bombal* merely refers to a process of modifying vectors in which selected scan operations are replaced by "pseudo-scan" operations, i.e., register accesses" in order to avoid actual scan circuitry. *Bombal*, col. 3, ll. 27-29. Thus, *Bombal* does not provide any teaching (or even suggestion) for selecting and automatically switching to remaining input or output lines via a selection signal. The section of *Bombal* which the Examiner relies on (FIG. 8, block 3) merely states that test patterns are generated for a second version using an automatic test pattern generation tool. Put more plainly, *Bombal* does not provide for changing the electrical input/output path along which a test signal is to be carried using a selection signal, and thus does not cure the deficiencies of *Watari* mentioned above. Accordingly, it is submitted that the combination of *Watari* and *Bombal* does not render obvious the subject matter of claims 5, 7 and 9.

With regard to the second rejection of claims 11-20 based on *Watari* and *Evans*, it is noted that independent claim 11 has been amended to recite that the plurality of input and output lines are positioned internally within the IC to be tested and that, if a test fails, remaining input and output lines are selected and automatically switched to using a selection signal.

It is submitted that the *Watari* and *Evans* references, as combined, fail to teach or suggest the subject matter of amended claim 11. As discussed above, the *Watari* reference does not teach or suggest using a selection signal to switch to remaining input or output lines. Moreover, the *Evans* reference does not teach selecting or switching between remaining input/output lines internal

to an IC under test (e.g., DUT 600 in FIG. 10 of *Evans*), but rather, appears to teach selecting different testing equipment on a rider board (112). For example, *Evans* states that "Input and output(I/O) nodes in the analog testing multiplexers 310 and the BERT [bit error rate testing] 312 are controlled via the multiplexer controller 306 to form signal paths . . . and to take signals off-board." *Evans*, pg. 5, paragraph 73. The multiplexing referred to in this passage is performed with respect to testing components located on the rider board that is coupled to but is also distinct from the device under test (600). Thus, the combination *Watari* and *Evans* does not teach or suggest selecting and switching internal input/output lines of an IC under test using a selection signal. It is accordingly submitted that that the combination of *Watari* and *Evans* does not render obvious the subject matter of independent claim 11 or its dependent claims 12-20.

For the foregoing reasons, withdrawal of the §103 rejections of claims 5, 7 and 9 based on *Watari* and *Bombal*, and of claims 11-20 based on *Watari* and *Evans*, is respectfully requested.

Conclusion

Applicants submit that all the pending claims are in allowable condition. It is also believed that no fees are due in conjunction with the amendment. However, if an Extension of Time is required to make this response timely, please accept this sentence as such a request and charge Deposit Account No. 04-1696 the requisite fee. If any other fees are required, please similarly charge Deposit Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney should any issues remain.

Respectfully Submitted,

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